Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A method for tuning over clock, for operating a system in an over clock state, comprising:
setting up a first time out and a second time out, wherein the first time out is greater than the second time out;
restarting the system to transfer the system from an initial stable state to an over clock state;
resetting the system and retaining a setting value of the system at the over clock state when the system is unable to stay in the over clock state within the second time out;
restarting the system with the setting value of the over clock state; and
restarting the system with a setting value of the initial stable state when the system is unable to stay in the over clock state within the first time out.

[c2] 2. The method for tuning over clock of claim 1, wherein the step of restarting the system to transfer the system from an initial stable state to an over clock state, further comprising changing an operating voltage of the system, such that the operating voltage of the system is higher than a voltage of the initial stable state.

[c3] 3. The method for tuning over clock of claim 1, wherein the step of restarting the system to transfer the system from an initial stable state to an over clock state, further comprising changing an operating frequency of the system, such that the operating frequency of the system is higher than a frequency of the initial stable state.

[c4] 4. An over clock tuning apparatus for operating a system operate in an over clock state, comprising:
a register, for storing a setting value which is used to set an over clock state;
a first timer, for calculating a first time out adapted for determining that the system is unable to transfer to the over clock state from a stable state of an initial value, wherein when the system is unable to stay in the over clock state within the first time out, the setting value of the over clock state is reset to the initial setting value, so as to restart the system;
a second timer, for calculating a second time out adapted for determining that the system is unable to stay in the over clock state, and the second time out is smaller than the first time out, wherein when the system is unable to stay in the over clock state within the second time out, a reset signal is generated and the setting value of the system at the over clock state is retained; and

a selection circuit, electrically coupled to the first timer and the second timer, for selecting the system to be restarted either with the initial setting value or with the over clock setting value.

[c5] 5. The over clock tuning apparatus of claim 4, wherein the selection circuit is an OR gate.

[c6] 6. The over clock tuning apparatus of claim 4, wherein the setting operation of the setting value of the system at the over clock state is performed by a BIOS.

[c7] 7. A tuning method for operating a system in a sub-stable state with high performance, comprising:
setting up a time out for determining that the system is unable to stay in a sub-stable state;
restarting the system with a setting value of the sub-stable state to transfer the system from an initial stable state to the sub-stable state;
restarting the system with the setting value of the sub-stable state when the system is unable to stay in the sub-stable state,; and
restarting the system with a setting value of the initial stable state when the time out is due and the system still cannot stay in the sub-stable state.

[c8] 8. The tuning method of claim 7, wherein the step of

restarting the system to transfer the system from an initial stable state to the sub-stable state, further comprising changing an operating voltage of the system, such that the operating voltage of the system is higher than a voltage of the initial stable state.

[c9] 9. The tuning method of claim 7, wherein the step of restarting the system to transfer the system from an initial stable state to the sub-stable state, further comprising changing an operating frequency of the system, such that the operating frequency of the system is higher than a frequency of the initial stable state.

[c10] 10. A method for tuning over clock for operating a system in an over clock state, comprising:
repeatedly restarting the system with a setting value of the over clock state within a predetermined period of time until the system can operate in the over clock state; and
restarting the system with a setting value of an initial state of the system when the predetermined period of time is due,.